Raritan PX2/PX3 Modbus Interface

Introduction

The PX2 device can act as a Modbus/TCP server. The Modbus service can be enabled in the Network Services section of the Device Settings menu in the web UI.

Supported Products

This document applies to the following product families:

- Raritan PX2, PX3, PXC and PXE intelligent PDUs
- Raritan PX3TS transfer switches
- Legrand intelligent PDUs
- Servertech PRO3X intelligent PDUs

Additionally this document describes the register set available at the main controller unit ID of Raritan BCM2 and PMC branch circuit monitors. **Note:** Only the Basic PDU Parameters and Peripheral Sensors sections apply to those products. The Modbus interface for power meters and panels is described in a separate document.

Supported Modbus Functions

The following Modbus function codes are supported:

- General Commands:
  - Read Device Identification (`2Bh`)
- Bit Access:
  - Read Coils (`01h`)
  - Write Single Coil (`05h`)
  - Write Multiple Coils (`0Fh`)
- 16-bit Word Access:
  - Read Holding Registers (`03h`)
  - Write Single Register (`06h`)
  - Write Multiple Registers (`10h`)
  - Mask Write Register (`16h`)

Feature Set

The following features of the PX2/PX3 are available via Modbus:

- Sensor readings for inlets and overcurrent protectors
- Outlet sensor readings (PX2-4K, PX2-5K, PX3-4K and PX3-5K series)
- Outlet control (PX2-2K, PX2-5K, PX3-2K, and PX3-5K series)
- Transfer switch status and control (PX3TS series)
- Peripheral sensor readings
- Peripheral actuator control

Register Layout

Conventions

- All register or coil addresses are hexadecimal, indicated by a h suffix.
- Data types which span multiple 16-bit registers are big-endian, i.e. the lowest register address contains the most significant bits.
- The following data types are supported for holding registers:
  - Word: 16-bit unsigned integer
  - DWord: 32-bit unsigned integer (two registers, big-endian)
  - QWord: 64-bit unsigned integer (four registers, big-endian)
  - Float: IEEE 32-bit floating point value (two registers, big-endian)
  - Bit Mask: 16 individual bits
- The access flags column can have the following values:
  - R: Read-only register
  - W: Write-only register (writing triggers an action, always reads 0)
  - R/W: Read-write register
- Reading a reserved register usually yields zero, but the meaning may change in future versions.
- Reserved bits in bit mask registers should always be written as 0.

Register Addresses and Numbers

The Modbus standard supports up to 65536 entities of each register type (input registers, holding register, coils, etc.). Entity addresses range from 0 to 65535 decimal (FFFFh hexadecimal). All register addresses listed in this document refer to these entity addresses.

Some Modbus software uses a 5- or 6-digit entity *number* convention where the first digit indicates the entity type:

Type	First Digit	5-Digit Numbers	6-Digit Numbers
Coil	0	00001 - 09999	000001 - 065536
Discrete Input	1	10001 - 19999	100001 - 165536
Input Register	3	30001 - 39999	300001 - 365536
Holding Register	4	40001 - 49999	400001 - 465536

Software packages using the 5-digit convention can only address 9999 entities of each type, so they can only access a limited range of the registers provided by the PX2/PX3 Modbus service. Most notably, the inlet and outlet register blocks are located outside of this range and cannot be accessed.

Software using the 6-digit convention can address all registers provided by the PX2/PX3 Modbus service.

To convert a holding register address from this document to a 5- or 6-digit register number, add 40001 or 400001 to the decimal value of the address. To convert a coil address from this document, just add 1. Some examples:

Register/Coil	Address (hex)	Address (dec)	5-Digit Number	6-Digit Number
Number of Outlets	0003h	3	40004	400004
Peripheral Sensor 4 Type	0830h	2096	42097	402096

Inlet 1 RMS Current	300Ah	12298	---	412299
Outlet 1 Relay Coil	0100h	256	00257	000257

Holding Register Map

Each PDU component (inlet, outlet, etc.) occupies a block of holding registers starting at a base address. See the referenced sections below for a description of registers inside each block.

Start	End	Function	See Section
0000h	0010h	Basic parameters, PDU layout	Basic PDU Parameters
...			
0800h	080Fh	Peripheral sensor 1	Peripheral Sensors
0810h	081Fh	Peripheral sensor 2	
...			
09F0h	09FFh	Peripheral sensor 32	
...			
2000h	20FFh	Transfer switch 1	Transfer Switch
...			
3000h	303Fh	Inlet 1	Inlets
3040h	306Fh	Inlet 1 pole 1	Poles
3070h	309Fh	Inlet 1 pole 2	
30A0h	30CFh	Inlet 1 pole 3	
30D0h	30FFh	Inlet 1 pole 4	
3100h	31FFh	Inlet 2 (incl. poles)	
...			
3F00h	3FFFh	Inlet 16 (incl. poles)	
4000h	403Fh	Overcurrent protector 1	Overcurrent Protectors
4040h	406Fh	OCP 1 pole 1	Poles
4070h	409Fh	OCP 1 pole 2	
40A0h	40CFh	OCP 1 pole 3	
40D0h	40FFh	OCP 1 pole 4	
4100h	41FFh	OCP 2 (incl. poles)	
...			
7F00h	7FFFh	OCP 64 (incl. poles)	
8000h	80FFh	Outlet 1	Outlets
8040h	806Fh	Outlet 1 pole 1	Poles
8070h	809Fh	Outlet 1 pole 2	
80A0h	80CFh	Outlet 1 pole 3	
80D0h	80FFh	Outlet 1 pole 4	
8100h	81FFh	Outlet 2 (incl. poles)	

...			
FF00h	FFFFh	Outlet 128 (incl. poles)	

Coil Map

Coils are used to reflect the trip status of overcurrent protectors or the relay control state of switched outlets.

Coil Address	Access	Function
0000h	R	Overcurrent protector 1 status
0001h	R	Overcurrent protector 2 status
...		
003Fh	R	Overcurrent protector 64 status
...		
0100h	R/W	Outlet 1 state
0101h	R/W	Outlet 2 state
...		
017Fh	R/W	Outlet 128 state

Basic PDU Parameters

Address	Type	Access	Parameter
0000h	Word	R	Register set version (8 bit major, 8 bit minor)
0001h	Word	R	Number of inlets
0002h	Word	R	Number of overcurrent protectors
0003h	Word	R	Number of outlets
0004h	Word	R	Number of transfer switches

Peripheral Sensors

Up to 32 peripheral sensors are supported. Each sensor occupies a block of 16 holding registers. The base address of a sensor's register block is determined by the following formula, with *i* being a sensor number between 0 and 31:

```
base address = 0800h + i * 10h
```

The full register address is determined by adding the offset from the table below to this base address. For example the reading of the third peripheral sensor (*i = 2*) is in register:

```
register address = base address    + offset
                 = 0800h + 2 * 10h + 02h
                 = 0822h (or 2082 decimal)
```

Offset	Type	Access	Parameter
00h	Word	R	Sensor type: • 0: unassigned • 1: Temperature in °C • 2: Relative humidity in % • 3: Air flow in m/s • 4: Air pressure in Pa • 5: Contact closure (0: off, 1: on) • 6: Vibration in G • 7: Water leak (0: normal, 1: alarm) • 8: Smoke detector (0: normal, 1: alarm) • 9: Ambient light in lux • 10: Dry contact (actuator, 0: off, 1: on) • 11: Magnetic contact (0: off, 1: on) • 12: Passive IR motion detector (0: off, 1: on) • 13: Tamper detector (0: normal, 1: alarm) • 14: Powered dry contact (actuator, 0: off, 1: on) • 15: Absolute humidity in g/m^3 • 16: Acceleration in G • 17: Door state (0: open, 1: closed) • 18: Door lock state (0: open, 1: closed) • 19: Door handle lock switch (0: open, 1: closed)
01h	Word	R	State (for discrete sensors)
02h - 03h	Float	R	Sensor reading (for numerical sensors, see above for unit)
04h	Word	R/W	Actuator control
05h - 0Fh			Reserved

Transfer Switch

For PX3TS models the transfer switch information is held in a register block starting at address 2000h.

Address	Type	Access	Parameter
2000h	Bit Mask	R	Transfer switch capabilities (supported sensors): • Bit 0: Inlet voltage phase difference sensor • Bits 1~15: Reserved
2001h	Word	R	Active inlet: • 0: No active inlet • 1: Inlet 1 • 2: Inlet 2
2002h	Word	R	Preferred inlet: • 1: Inlet 1 • 2: Inlet 2
2003h	Word	W	Transfer to inlet. If the new inlet is available, it will become both active and preferred. • Bits 0~30: New active inlet (1 or 2) • Bit 31: Force switch even if the phase difference between the inlets is too large
2004h	Bit Mask	R	Fault flags: • Bit 0: Inlet phases out of sync • Bit 1: Overload alarm • Bits 2~15: Reserved
2005h	Bit Mask	R	Inlet 1 fault flags: • Bit 0: +12 V power supply fault • Bit 1: Fuse blown • Bit 2: MOV surge protector fault • Bit 3: Switch open • Bit 4: Switch short • Bits 5~15: Reserved
2006h	Bit Mask	R	Inlet 2 fault flags (see above)
2007h			Reserved
2008h - 2009h	Float	R	Inlet phase sync angle in degrees
200Ah - 201Fh			Reserved

2020h	Bit Mask	R/W	Transfer settings: • Bit 0: Enable automatic retransfer • Bit 1: Suppress automatic retransfer on phase sync alarm • Bit 2: Enable manual transfer front panel button • Bits 3~15: Reserved
2021h	Word	R/W	Automatic retransfer wait time in seconds
2022h	Bit Mask	R/W	Inlet 1 enabled voltage thresholds: • Bit 0: Lower critical threshold enabled • Bit 1: Lower warning threshold enabled • Bit 2: Upper warning threshold enabled • Bit 3: Upper critical threshold enabled • Bits 4~15: Reserved
2023h	Word	R/W	Inlet 1 lower critical voltage threshold (0.01 V)
2024h	Word	R/W	Inlet 1 lower warning voltage threshold (0.01 V)
2025h	Word	R/W	Inlet 1 upper warning voltage threshold (0.01 V)
2026h	Word	R/W	Inlet 1 upper critical voltage threshold (0.01 V)
2027h	Word	R/W	Inlet 1 voltage assertion timeout (seconds)
2028h	Word	R/W	Inlet 1 voltage deassertion hysteresis (0.01 V)
2029h	Bit Mask	R/W	Inlet 1 enabled frequency thresholds: • Bit 0: Lower critical threshold enabled • Bit 1: Lower warning threshold enabled • Bit 2: Upper warning threshold enabled • Bit 3: Upper critical threshold enabled • Bits 4~15: Reserved
202Ah	Word	R/W	Inlet 1 lower critical frequency threshold (0.01 Hz)
202Bh	Word	R/W	Inlet 1 lower warning frequency threshold (0.01 Hz)
202Ch	Word	R/W	Inlet 1 upper warning frequency threshold (0.01 Hz)
202Dh	Word	R/W	Inlet 1 upper critical frequency threshold (0.01 Hz)
202Eh	Word	R/W	Inlet 1 frequency assertion timeout (seconds)
202Fh	Word	R/W	Inlet 1 frequency deassertion hysteresis (0.01 Hz)
2030h	Bit Mask	R/W	Inlet 2 enabled voltage thresholds: • Bit 0: Lower critical threshold enabled • Bit 1: Lower warning threshold enabled • Bit 2: Upper warning threshold enabled • Bit 3: Upper critical threshold enabled • Bits 4~15: Reserved
2031h	Word	R/W	Inlet 2 lower critical voltage threshold (0.01 V)

2032h	Word	R/W	Inlet 2 lower warning voltage threshold (0.01 V)
2033h	Word	R/W	Inlet 2 upper warning voltage threshold (0.01 V)
2034h	Word	R/W	Inlet 2 upper critical voltage threshold (0.01 V)
2035h	Word	R/W	Inlet 2 voltage assertion timeout (seconds)
2036h	Word	R/W	Inlet 2 voltage deassertion hysteresis (0.01 V)
2037h	Bit Mask	R/W	Inlet 2 enabled frequency thresholds: • Bit 0: Lower critical threshold enabled • Bit 1: Lower warning threshold enabled • Bit 2: Upper warning threshold enabled • Bit 3: Upper critical threshold enabled • Bits 4~15: Reserved
2038h	Word	R/W	Inlet 2 lower critical frequency threshold (0.01 Hz)
2039h	Word	R/W	Inlet 2 lower warning frequency threshold (0.01 Hz)
203Ah	Word	R/W	Inlet 2 upper warning frequency threshold (0.01 Hz)
203Bh	Word	R/W	Inlet 2 upper critical frequency threshold (0.01 Hz)
203Ch	Word	R/W	Inlet 2 frequency assertion timeout (seconds)
203Dh	Word	R/W	Inlet 2 frequency deassertion hysteresis (0.01 Hz)
203Eh - 20FFh			Reserved

Inlets

Up to 16 inlets are supported. Each inlet occupies a block of 256 holding registers. The base address of an inlet's register block is determined by the following formula, with *i* being an inlet number between 0 and 15:

```
base address = 3000h + i * 100h
```

The full register address is determined by adding the offset from the table below to this base address. For example the line frequency of the first inlet (*i = 0*) is in register:

```
register address = base address       + offset
                 = 3000h + 0 * 100h   + 22h
                 = 3022h (or 12322 decimal)
```

The sensor readings listed in the table are inlet-global readings. In case of three-phase inlets the per-phase readings can be found in the pole blocks starting at offsets `40h`, `70h`, `A0h` and `D0h`. See section Poles below for details.

Offset	Type	Access	Parameter
`00h`	Bit Mask	R	Inlet capabilities (supported sensors): • Bit 0: RMS voltage • Bit 1: RMS current • Bit 2: Peak current • Bit 3: Reserved • Bit 4: Unbalanced current • Bit 5: Active power • Bit 6: Apparent power • Bit 7: Power factor • Bit 8: Active energy counter • Bit 9: Apparent energy counter • Bit 10: Phase angle • Bit 11: Line frequency • Bit 12: Reactive power • Bit 13: Reactive energy counter • Bit 14: Power quality • Bit 15: Surge protector status
`01h`	Bit Mask	R	Inlet capabilities (continued): • Bit 0: Residual current • Bit 1: Residual DC current • Bits 2~15: Reserved
`02h`	Word	R	Number of inlet poles
`03h`	Word	R	Minimum voltage rating in V
`04h`	Word	R	Maximum voltage rating in V

05h	Word	R	Current rating in A
06h - 07h			Reserved
08h - 09h	Float	R	RMS voltage reading in V
0Ah - 0Bh	Float	R	RMS current reading in A
0Ch - 0Fh			Reserved
10h - 11h	Float	R	Unbalanced current reading in %
12h - 13h	Float	R	Active power reading in W
14h - 15h	Float	R	Apparent power reading in VA
16h - 17h	Float	R	Power factor reading (no unit)
18h - 1Bh	QWord	R	Active energy counter in Wh
1Ch - 1Fh	QWord	R	Apparent energy counter in VAh
20h - 21h	Float	R	Phase angle between voltage and current in degrees
22h - 23h	Float	R	Line frequency reading in Hz
24h - 25h	Float	R	Reactive power reading in var
26h - 29h	QWord	R	Reactive energy counter in varh
2Ah	Word	R	Power quality: • 0: Unknown • 1: Normal • 2: Warning • 3: Critical
2Bh - 2Fh			Reserved
30h	Word	R	Surge protector status: • 0: OK • 1: Alarm
31h	Word	R	Residual current status: • 0: Unknown • 1: Normal • 2: Warning • 3: Critical • 4: Self-Test • 5: Failure
32h - 33h	Float	R	Residual current reading in A
34h - 35h	Float	R	Residual DC current reading in A
36h - 3Fh			Reserved
40h - 6Fh			Pole 1 (see Poles)
70h - 9Fh			Pole 2
A0h - CFh			Pole 3
D0h - FFh			Pole 4

Overcurrent Protectors

Up to 64 overcurrent protectors (OCP) are supported. Each OCP occupies a block of 256 holding registers. The base address of an OCP's register block is determined by the following formula, with *i* being an OCP number between 0 and 63:

```
base address = 4000h + i * 100h
```

The full register address is determined by adding the offset from the table below to this base address. For example the RMS current reading of the fourth OCP (*i* = *3*) is in register:

```
register address = base address     + offset
                 = 4000h + 3 * 100h + 0Ah
                 = 430Ah (or 17162 decimal)
```

The OCP trip states are reflected in a coils ranging from `0000h` (OCP 1) to `003Fh` (OCP 64). A coil value of 1 indicates a closed (good) OCP, a coil value of 0 indicates an open (tripped) OCP. Trip status coils are read-only.

Offset	Type	Access	Parameter
`00h`	Bit Mask	R	Capabilities (supported sensors): • Bit 0: Reserved • Bit 1: RMS current • Bit 2: Peak current • Bits 3~14: Reserved • Bit 15: Trip detection
`01h`			Reserved
`02h`	Word	R	Number of overcurrent protector poles
`03h - 04h`			Reserved
`05h`	Word	R	Current rating in A
`06h - 09h`			Reserved
`0Ah - 0Bh`	Float	R	RMS current reading in A
`0Ch - 0Dh`	Float	R	Peak current reading in A
`0Eh - 3Fh`			Reserved
`40h - 6Fh`			Pole 1 (see Poles)
`70h - 9Fh`			Pole 2
`A0h - CFh`			Pole 3
`D0h - FFh`			Pole 4

Outlets

Up to 128 outlets are supported. Each outlet occupies a block of 256 holding registers. The base address of an outlet's register block is determined by the following formula, with *i* being an outlet number between 0 and 127:

```
base address = 8000h + i * 100h
```

The full register address is determined by adding the offset from the table below to this base address. For example the RMS current reading of the fourth outlet (*i = 3*) is in register:

```
register address = base address     + offset
                 = 8000h + 3 * 100h + 0Ah
                 = 830Ah (or 33546 decimal)
```

In case of switched outlets the relay status is reflected and can be controlled by reading or writing a coil. Outlet coil addresses range from `0100h` (outlet 1) to `017Fh` (outlet 128). A coil value of 1 indicates the outlet is switched on, a coil value of 0 indicates the outlet is switched off. Whether or not an outlet is switched can be determined by checking bit 15 of the respective outlet's capabilities register.

Offset	Type	Access	Parameter
`00h`	Bit Mask	R	Outlet capabilities (supported sensors): • Bit 0: RMS voltage • Bit 1: RMS current • Bits 2~3: Reserved • Bit 4: Unbalanced current • Bit 5: Active power • Bit 6: Apparent power • Bit 7: Power factor • Bit 8: Active energy counter • Bit 9: Apparent energy counter • Bit 10: Phase angle • Bit 11: Line frequency • Bit 12: Reactive power • Bit 13: Reactive energy counter • Bit 14: Reserved • Bit 15: Outlet control coil (switchable)
`01h`			Reserved
`02h`	Word	R	Number of outlet poles
`03h`	Word	R	Minimum voltage rating in V
`04h`	Word	R	Maximum voltage rating in V
`05h`	Word	R	Current rating in A
`06h - 07h`			Reserved
`08h - 09h`	Float	R	RMS voltage reading in V

0Ah - 0Bh	Float	R	RMS current reading in A
0Ch - 0Fh			Reserved
10h - 11h	Float	R	Unbalanced current reading in %
12h - 13h	Float	R	Active power reading in W
14h - 15h	Float	R	Apparent power reading in VA
16h - 17h	Float	R	Power factor reading (no unit)
18h - 1Bh	QWord	R	Active energy counter in Wh
1Ch - 1Fh	QWord	R	Apparent energy counter in VAh
20h - 21h	Float	R	Phase angle between voltage and current in degrees
22h - 23h	Float	R	Line frequency reading in Hz
24h - 25h	Float	R	Reactive power reading in var
26h - 29h	QWord	R	Reactive energy counter in varh
2Ah - 3Fh			Reserved
40h - 6Fh			Pole 1 (see Poles)
70h - 9Fh			Pole 2
A0h - CFh			Pole 3
D0h - FFh			Pole 4

Poles

Poles contain per-line sensor readings for multi-phase inlets or outlets. They are embedded in the holding register blocks listed above. The number of poles for an inlet out outlet can be found at register offset `02h` in the respective block.

The base addresses for inlet *i* poles are (*i=0..15*):

- Pole count: `3002h + i * 100h`
- Pole 1: `3040h + i * 100h`
- Pole 2: `3070h + i * 100h`
- Pole 3: `30A0h + i * 100h`
- Pole 4: `30D0h + i * 100h`

The base addresses for outlet *i* pole blocks are (*i=0..127*):

- Pole count: `8002h + i * 100h`
- Pole 1: `8040h + i * 100h`
- Pole 2: `8070h + i * 100h`
- Pole 3: `80A0h + i * 100h`
- Pole 4: `80D0h + i * 100h`

Offset	Type	Access	Parameter
`00h`	Bit Mask	R	Pole capabilities (supported sensors): • Bit 0: RMS voltage • Bit 1: RMS current • Bit 2: Peak current • Bits 3~4: Reserved • Bit 5: Active power • Bit 6: Apparent power • Bit 7: Power factor • Bit 8: Active energy counter • Bit 9: Apparent energy counter • Bit 10: Phase angle • Bit 11: Line frequency • Bit 12: Reactive power • Bit 13: Reactive energy counter • Bit 14: Residual current • Bit 15: Residual DC current
`01h - 07h`			Reserved
`08h - 09h`	Float	R	RMS voltage reading in V
`0Ah - 0Bh`	Float	R	RMS current reading in A
`0Ch - 11h`			Reserved

12h - 13h	Float	R	Active power reading in W
14h - 15h	Float	R	Apparent power reading in VA
16h - 17h	Float	R	Power factor reading (no unit)
18h - 1Bh	QWord	R	Active energy counter in Wh
1Ch - 1Fh	QWord	R	Apparent energy counter in VAh
20h - 21h	Float	R	Phase angle between voltage and current in degrees
22h - 23h	Float	R	Line frequency reading in Hz
24h - 25h	Float	R	Reactive power reading in var
26h - 29h	QWord	R	Reactive energy counter in varh
2Ah	Word	R	Residual current status: • 0: Unknown • 1: Normal • 2: Warning • 3: Critical • 4: Self-Test • 5: Failure
2Bh - 2Ch	Float	R	Residual current reading in A
2Dh - 2Eh	Float	R	Residual DC current reading in A
2Fh			Reserved