

# Raritan PX2/PX3 Modbus Interface

## Contents

<b>Introduction</b>	<b>2</b>
Supported Modbus Functions . . . . .	2
Feature Set . . . . .	2
<b>Register Layout</b>	<b>3</b>
Conventions . . . . .	3
Holding Register Map . . . . .	3
Coil Map . . . . .	4
Basic PDU Parameters . . . . .	4
Peripheral Sensors . . . . .	6
Transfer Switches . . . . .	9
Inlets . . . . .	15
Overcurrent Protectors . . . . .	19
Outlets . . . . .	20
Poles . . . . .	23

## Introduction

The PX2 device can act as a Modbus/TCP server. The Modbus service can be enabled in the Network Services section of the Device Settings menu in the web UI.

## Supported Modbus Functions

The following Modbus function codes are supported:

- General Commands:
  - Read Device Identification (0x2b)
- Bit Access:
  - Read Coils (0x01)
  - Write Coils (0x05)
  - Write Multiple Coils (0x0f)
- 16-bit Word Access:
  - Read Holding Registers (0x03)
  - Write Single Register (0x06)
  - Write Multiple Registers (0x10)
  - Mask Write Register (0x16)

## Feature Set

The following features of the PX2/PX3 are available via Modbus:

- Sensor readings for inlets and overcurrent protectors
- Outlet sensor readings (PX2-4K, PX2-5K, PX3-4K and PX3-5K series)
- Outlet control (PX2-2K, PX2-5K, PX3-2K, and PX3-5K series)
- Transfer switch status and control (PX3TS series)
- Peripheral sensor readings
- Peripheral actuator control

# Register Layout

## Conventions

- All register or coil addresses are hexadecimal, indicated by a 0x prefix.
- Data types which span multiple 16-bit registers are big-endian, i.e. the lowest register address contains the most significant bits.
- The following data types are supported for holding registers:
  - Word: 16-bit unsigned integer
  - DWord: 32-bit unsigned integer (two registers, big-endian)
  - QWord: 64-bit unsigned integer (four registers, big-endian)
  - Float: IEEE 32-bit floating point value (two registers, big-endian)
  - Bit Mask: 16 individual bits
- The access flags column can have the following values:
  - R: Read-only register
  - W: Write-only register (writing triggers an action, always reads 0)
  - R/W: Read-write register
- Reading a reserved register usually yields zero, but the meaning may change in future versions.
- Reserved bits in bit mask registers should always be written as 0.

## Holding Register Map

Start	End	Function	See Section
0x0000	0x0010	Basic parameters, PDU layout	Basic PDU Parameters
...			
0x0800	0x080f	Peripheral sensor 1	Peripheral Sensors
0x0810	0x081f	Peripheral sensor 2	
...			
0x09f0	0x09ff	Peripheral sensor 32	
...			
0x2000	0x20ff	Transfer switch 1	Transfer Switches
0x2100	0x21ff	Transfer switch 2	
...			
0x2f00	0x2fff	Transfer switch 16	
0x3000	0x303f	Inlet 1	Inlets
0x3040	0x306f	Inlet 1 pole 1	Poles
0x3070	0x309f	Inlet 1 pole 2	
0x30a0	0x30cf	Inlet 1 pole 3	
0x30d0	0x30ff	Inlet 1 pole 4	
0x3100	0x31ff	Inlet 2 (incl. poles)	

Start	End	Function	See Section
...			
0x3f00	0x3fff	Inlet 16 (incl. poles)	
0x4000	0x403f	Overcurrent protector 1	Overcurrent Protectors Poles
0x4040	0x406f	OCP 1 pole 1	
0x4070	0x409f	OCP 1 pole 2	
0x40a0	0x40cf	OCP 1 pole 3	
0x40d0	0x40ff	OCP 1 pole 4	
0x4100	0x41ff	OCP 2 (incl. poles)	
...			
0x7f00	0x7fff	OCP 64 (incl. poles)	
0x8000	0x80ff	Outlet 1	Outlets
0x8040	0x806f	Outlet 1 pole 1	Poles
0x8070	0x809f	Outlet 1 pole 2	
0x80a0	0x80cf	Outlet 1 pole 3	
0x80d0	0x80ff	Outlet 1 pole 4	
0x8100	0x81ff	Outlet 2 (incl. poles)	
...			
0xff00	0xffff	Outlet 128 (incl. poles)	

## Coil Map

Coil Address	Access	Function
0x0000	R	Overcurrent protector 1 status
0x0001	R	Overcurrent protector 2 status
...		
0x003f	R	Overcurrent protector 64 status
...		
0x0100	R/W	Outlet 1 state
0x0101	R/W	Outlet 2 state
...		
0x017f	R/W	Outlet 128 state

## Basic PDU Parameters

---

Address	Type	Access	Parameter
0x0000	Word	R	Register set version (8 bit major, 8 bit minor)
0x0001	Word	R	Number of inlets
0x0002	Word	R	Number of overcurrent protectors
0x0003	Word	R	Number of outlets
0x0004	Word	R	Number of transfer switches

---

## Peripheral Sensors

- Up to 32 sensors, 16 holding registers each
- Base address ( $i = 0..31$ ):  $0x0800 + i * 0x0010$

Offset	Type	Access	Parameter
0x00	Word	R	Sensor type: <ul style="list-style-type: none"> <li>• 0: unassigned</li> <li>• 1: Temperature in degrees Celsius</li> <li>• 2: Relative humidity in %</li> <li>• 3: Air flow in m/s</li> <li>• 4: Air pressure in Pa</li> <li>• 5: Contact closure (0: off, 1: on)</li> <li>• 6: Vibration in G</li> <li>• 7: Water leak (0: normal, 1: alarm)</li> <li>• 8: Smoke detector (0: normal, 1: alarm)</li> <li>• 9: Ambient light in lux</li> <li>• 10: Dry contact (actuator, 0: off, 1: on)</li> <li>• 11: Magnetic contact (0: off, 1: on)</li> <li>• 12: Passive IR motion detector (0: off, 1: on)</li> <li>• 13: Tamper detector (0: normal, 1: alarm)</li> <li>• 14: Powered dry contact (actuator, 0: off, 1: on)</li> <li>• 15: Absolute humidity in g/m<sup>3</sup></li> <li>• 16: Acceleration</li> </ul>

Offset	Type	Access	Parameter
0x01	Word	R	State (for discrete sensors)
0x02~0x03	Float	R	Sensor reading (for numerical sensors, see above for unit)
0x04	Word	R/W	Actuator control
0x05~0x0f			Reserved



## Transfer Switches

- Up to 16 transfer switches, 256 holding registers each
- Base address ( $i = 0..15$ ):  $0x2000 + i * 0x0100$

Offset	Type	Access	Parameter
0x00	Bit Mask	R	Transfer switch capabilities (supported sensors): <ul style="list-style-type: none"> <li>• Bit 0: Inlet voltage phase difference sensor</li> <li>• Bits 1~15: Reserved</li> </ul>
0x01	Word	R	Selected inlet: <ul style="list-style-type: none"> <li>• 0: No active inlet</li> <li>• 1: Inlet 1</li> <li>• 2: Inlet 2</li> </ul>
0x02	Word	R	Preferred inlet: <ul style="list-style-type: none"> <li>• 1: Inlet 1</li> <li>• 2: Inlet 2</li> </ul>
0x03	Word	W	Transfer to inlet. If the new inlet is available, it will become both active and preferred. <ul style="list-style-type: none"> <li>• Bits 0~30: New active inlet (1 or 2)</li> <li>• Bit 31: Force switch even if the phase difference between the inlets is too large</li> </ul>

Offset	Type	Access	Parameter
0x04	Bit Mask	R	Fault flags: <ul style="list-style-type: none"> <li>• Bit 0: Inlet phases out of sync</li> <li>• Bit 1: Overload alarm</li> <li>• Bits 2~15: Reserved</li> </ul>
0x05	Bit Mask	R	Inlet 1 fault flags: <ul style="list-style-type: none"> <li>• Bit 0: +12 V power supply fault</li> <li>• Bit 1: Fuse blown</li> <li>• Bit 2: MOV surge protector fault</li> <li>• Bit 3: Switch open</li> <li>• Bit 4: Switch short</li> <li>• Bits 5~15: Reserved</li> </ul>
0x06	Bit Mask	R	Inlet 2 fault flags (see above)
0x07			Reserved
0x08~0x09	Float	R	Inlet voltage phase difference in degrees
0x0a~0x1f			Reserved

Offset	Type	Access	Parameter
0x20	Bit Mask	R/W	Transfer settings: <ul style="list-style-type: none"> <li>• Bit 0: Enable automatic retransfer</li> <li>• Bit 1: Suppress automatic retransfer on phase sync alarm</li> <li>• Bit 2: Enable manual transfer front panel button</li> <li>• Bits 3~15: Reserved</li> </ul>
0x21	Word	R/W	Automatic retransfer wait time in seconds
0x22	Bit Mask	R/W	Inlet 1 enabled voltage thresholds: <ul style="list-style-type: none"> <li>• Bit 0: Lower critical threshold enabled</li> <li>• Bit 1: Lower warning threshold enabled</li> <li>• Bit 2: Upper warning threshold enabled</li> <li>• Bit 3: Upper critical threshold enabled</li> <li>• Bits 4~15: Reserved</li> </ul>
0x23	Word	R/W	Inlet 1 lower critical voltage threshold (0.01 V)

Offset	Type	Access	Parameter
0x24	Word	R/W	Inlet 1 lower warning voltage threshold (0.01 V)
0x25	Word	R/W	Inlet 1 upper warning voltage threshold (0.01 V)
0x26	Word	R/W	Inlet 1 upper critical voltage threshold (0.01 V)
0x27	Word	R/W	Inlet 1 voltage assertion timeout (seconds)
0x28	Word	R/W	Inlet 1 voltage deassertion hysteresis (0.01 V)
0x29	Bit Mask	R/W	Inlet 1 enabled frequency thresholds: <ul style="list-style-type: none"> <li>• Bit 0: Lower critical threshold enabled</li> <li>• Bit 1: Lower warning threshold enabled</li> <li>• Bit 2: Upper warning threshold enabled</li> <li>• Bit 3: Upper critical threshold enabled</li> <li>• Bits 4~15: Reserved</li> </ul>
0x2a	Word	R/W	Inlet 1 lower critical frequency threshold (0.01 Hz)
0x2b	Word	R/W	Inlet 1 lower warning frequency threshold (0.01 Hz)
0x2c	Word	R/W	Inlet 1 upper warning frequency threshold (0.01 Hz)
0x2d	Word	R/W	Inlet 1 upper critical frequency threshold (0.01 Hz)
0x2e	Word	R/W	Inlet 1 frequency assertion timeout (seconds)
0x2f	Word	R/W	Inlet 1 frequency deassertion hysteresis (0.01 Hz)

Offset	Type	Access	Parameter
0x30	Bit Mask	R/W	Inlet 2 enabled voltage thresholds: <ul style="list-style-type: none"> <li>• Bit 0: Lower critical threshold enabled</li> <li>• Bit 1: Lower warning threshold enabled</li> <li>• Bit 2: Upper warning threshold enabled</li> <li>• Bit 3: Upper critical threshold enabled</li> <li>• Bits 4~15: Reserved</li> </ul>
0x31	Word	R/W	Inlet 2 lower critical voltage threshold (0.01 V)
0x32	Word	R/W	Inlet 2 lower warning voltage threshold (0.01 V)
0x33	Word	R/W	Inlet 2 upper warning voltage threshold (0.01 V)
0x34	Word	R/W	Inlet 2 upper critical voltage threshold (0.01 V)
0x35	Word	R/W	Inlet 2 voltage assertion timeout (seconds)
0x36	Word	R/W	Inlet 2 voltage deassertion hysteresis (0.01 V)

Offset	Type	Access	Parameter
0x37	Bit Mask	R/W	Inlet 2 enabled frequency thresholds: <ul style="list-style-type: none"> <li>• Bit 0: Lower critical threshold enabled</li> <li>• Bit 1: Lower warning threshold enabled</li> <li>• Bit 2: Upper warning threshold enabled</li> <li>• Bit 3: Upper critical threshold enabled</li> <li>• Bits 4~15: Reserved</li> </ul>
0x38	Word	R/W	Inlet 2 lower critical frequency threshold (0.01 Hz)
0x39	Word	R/W	Inlet 2 lower warning frequency threshold (0.01 Hz)
0x3a	Word	R/W	Inlet 2 upper warning frequency threshold (0.01 Hz)
0x3b	Word	R/W	Inlet 2 upper critical frequency threshold (0.01 Hz)
0x3c	Word	R/W	Inlet 2 frequency assertion timeout (seconds)
0x3d	Word	R/W	Inlet 2 frequency deassertion hysteresis (0.01 Hz)
0x3e~0xff			Reserved

## Inlets

- Up to 16 inlets, 256 holding registers each
- Base address ( $i = 0..15$ ):  $0x3000 + i * 0x0100$

Offset	Type	Access	Parameter
0x00	Bit Mask	R	Inlet capabilities (supported sensors): <ul style="list-style-type: none"> <li>• Bit 0: RMS voltage</li> <li>• Bit 1: RMS current</li> <li>• Bits 3~4: Reserved</li> <li>• Bit 4: Unbalanced current</li> <li>• Bit 5: Active power</li> <li>• Bit 6: Apparent power</li> <li>• Bit 7: Power factor</li> <li>• Bit 8: Active energy counter</li> <li>• Bit 9: Apparent energy counter</li> <li>• Bit 10: Phase angle</li> <li>• Bit 11: Line frequency</li> <li>• Bit 12: Reactive power</li> <li>• Bit 13: Reactive energy counter</li> <li>• Bit 14: Power quality</li> <li>• Bit 15: Surge protector status</li> </ul>



Offset	Type	Access	Parameter
0x01	Bit Mask	R	Inlet capabilities (continued): <ul style="list-style-type: none"> <li>• Bit 0: Residual current</li> <li>• Bit 1: Residual DC current</li> <li>• Bits 2~15: Reserved</li> </ul>
0x02	Word	R	Number of inlet poles
0x03	Word	R	Minimum voltage rating in V
0x04	Word	R	Maximum voltage rating in V
0x05	Word	R	Current rating in A
0x06~0x07			Reserved
0x08~0x09	Float	R	RMS voltage reading in V
0x0a~0x0b	Float	R	RMS current reading in A
0x0c~0x0f			Reserved
0x10~0x11	Float	R	Unbalanced current reading in %
0x12~0x13	Float	R	Active power reading in W
0x14~0x15	Float	R	Apparent power reading in VA
0x16~0x17	Float	R	Power factor reading (no unit)
0x18~0x1b	QWord	R	Active energy counter in Wh
0x1c~0x1f	QWord	R	Apparent energy counter in VAh
0x20~0x21	Float	R	Phase angle between voltage and current in degrees
0x22~0x23	Float	R	Line frequency reading in Hz
0x24~0x25	Float	R	Reactive power reading in var
0x26~0x29	QWord	R	Reactive energy counter in varh
0x2a	Word	R	Power quality: <ul style="list-style-type: none"> <li>• 0: Unknown</li> <li>• 1: Normal</li> <li>• 2: Warning</li> <li>• 3: Critical</li> </ul>
0x2b~0x2f			Reserved
0x30	Word	R	Surge protector status: <ul style="list-style-type: none"> <li>• 0: OK</li> <li>• 1: Alarm</li> </ul>

Offset	Type	Access	Parameter
0x31	Word	R	Residual current status: <ul style="list-style-type: none"> <li>• 0: Unknown</li> <li>• 1: Normal</li> <li>• 2: Warning</li> <li>• 3: Critical</li> <li>• 4: Self-Test</li> <li>• 5: Failure</li> </ul>
0x32~0x33	Float	R	Residual current reading in A
0x34~0x35	Float	R	Residual DC current reading in A
0x36~0x3f			Reserved
0x40~0x6f			Pole 1 (see section Poles)
0x70~0x9f			Pole 2
0xa0~0xcf			Pole 3
0xd0~0xff			Pole 4

## Overcurrent Protectors

- Up to 64 overcurrent protectors, 256 holding registers each
- Base address ( $i = 0..63$ ):  $0x4000 + i * 0x0100$
- Trip status is represented by coils  $0x0000$  to  $0x003f$  (0 = open, 1 = closed)

Offset	Type	Access	Parameter
0x00	Bit Mask	R	Capabilities (supported sensors): <ul style="list-style-type: none"> <li>• Bit 0: Reserved</li> <li>• Bit 1: RMS current</li> <li>• Bit 2: Peak current</li> <li>• Bits 3~14: Reserved</li> <li>• Bit 15: Trip detection</li> </ul>
0x01			Reserved
0x02	Word	R	Number of overcurrent protector poles
0x03~0x04			Reserved
0x05	Word	R	Current rating in A
0x06~0x09			Reserved
0x0a~0x0b	Float	R	RMS current reading in A
0x0c~0x0d	Float	R	Peak current reading in A
0x0e~0x3f			Reserved
0x40~0x6f			Pole 1 (see section Poles)
0x70~0x9f			Pole 2
0xa0~0xcf			Pole 3
0xd0~0xff			Pole 4

## Outlets

- Up to 128 outlets, 256 holding registers each
- Base address ( $i = 0..127$ ):  $0x8000 + i * 0x0100$
- Outlet state (for switchable units) is controlled by coils  $0x0100$  to  $0x017f$   
(0 = off, 1 = on)

Offset	Type	Access	Parameter
0x00	Bit Mask	R	Outlet capabilities (supported sensors): <ul style="list-style-type: none"> <li>• Bit 0: RMS voltage</li> <li>• Bit 1: RMS current</li> <li>• Bits 2~3: Reserved</li> <li>• Bit 4: Unbalanced current</li> <li>• Bit 5: Active power</li> <li>• Bit 6: Apparent power</li> <li>• Bit 7: Power factor</li> <li>• Bit 8: Active energy counter</li> <li>• Bit 9: Apparent energy counter</li> <li>• Bit 10: Phase angle</li> <li>• Bit 11: Line frequency</li> <li>• Bit 12: Reactive power</li> <li>• Bit 13: Reactive energy counter</li> <li>• Bit 14: Reserved</li> <li>• Bit 15: Outlet control coil (switchable)</li> </ul>

Offset	Type	Access	Parameter
0x01			Reserved
0x02	Word	R	Number of outlet poles
0x03	Word	R	Minimum voltage rating in V
0x04	Word	R	Maximum voltage rating in V
0x05	Word	R	Current rating in A
0x06~0x07			Reserved
0x08~0x09	Float	R	RMS voltage reading in V
0x0a~0x0b	Float	R	RMS current reading in A
0x0c~0x0f			Reserved
0x10~0x11	Float	R	Unbalanced current reading in %
0x12~0x13	Float	R	Active power reading in W
0x14~0x15	Float	R	Apparent power reading in VA
0x16~0x17	Float	R	Power factor reading (no unit)
0x18~0x1b	QWord	R	Active energy counter in Wh
0x1c~0x1f	QWord	R	Apparent energy counter in VAh
0x20~0x21	Float	R	Phase angle between voltage and current in degrees
0x22~0x23	Float	R	Line frequency reading in Hz
0x24~0x25	Float	R	Reactive power reading in var
0x26~0x29	QWord	R	Reactive energy counter in varh
0x2a~0x3f			Reserved
0x40~0x6f			Pole 1 (see section Poles)
0x70~0x9f			Pole 2
0xa0~0xcf			Pole 3
0xd0~0xff			Pole 4

## Poles

- Embedded into the register space of inlets, overcurrent protectors and outlets
- The number of poles depends on the pole count register at offset 0x02
- Base addresses for inlet  $i$  pole blocks ( $i=0..15$ ):
  - Pole count:  $0x3002 + i * 0x1000$
  - Pole 1:  $0x3040 + i * 0x0100$
  - Pole 2:  $0x3070 + i * 0x0100$
  - Pole 3:  $0x30a0 + i * 0x0100$
  - Pole 4:  $0x30d0 + i * 0x0100$
- Base addresses for overcurrent protector  $i$  pole blocks ( $i=0..63$ ):
  - Pole count:  $0x4002 + i * 0x1000$
  - Pole 1:  $0x4040 + i * 0x0100$
  - Pole 2:  $0x4070 + i * 0x0100$
  - Pole 3:  $0x40a0 + i * 0x0100$
  - Pole 4:  $0x40d0 + i * 0x0100$
- Base addresses for outlet  $i$  pole blocks ( $i=0..127$ ):
  - Pole count:  $0x8002 + i * 0x1000$
  - Pole 1:  $0x8040 + i * 0x0100$
  - Pole 2:  $0x8070 + i * 0x0100$
  - Pole 3:  $0x80a0 + i * 0x0100$
  - Pole 4:  $0x80d0 + i * 0x0100$

Offset	Type	Access	Parameter
0x00	Bit Mask	R	Pole capabilities (supported sensors): <ul style="list-style-type: none"> <li>• Bit 0: RMS voltage</li> <li>• Bit 1: RMS current</li> <li>• Bits 2-4: Reserved</li> <li>• Bit 5: Active power</li> <li>• Bit 6: Apparent power</li> <li>• Bit 7: Power factor</li> <li>• Bit 8: Active energy counter</li> <li>• Bit 9: Apparent energy counter</li> <li>• Bit 10: Phase angle</li> <li>• Bit 11: Line frequency</li> <li>• Bit 12: Reactive power</li> <li>• Bit 13: Reactive energy counter</li> <li>• Bit 14: Residual current</li> <li>• Bit 15: Residual DC current</li> </ul>
0x01~0x07			Reserved
0x08~0x09	Float	R	RMS voltage reading in V
0x0a~0x0b	Float	R	RMS current reading in A



Offset	Type	Access	Parameter
0x0c~0x11			Reserved
0x12~0x13	Float	R	Active power reading in W
0x14~0x15	Float	R	Apparent power reading in VA
0x16~0x17	Float	R	Power factor reading (no unit)
0x18~0x1b	QWord	R	Active energy counter in Wh
0x1c~0x1f	QWord	R	Apparent energy counter in VAh
0x20~0x21	Float	R	Phase angle between voltage and current in degrees
0x22~0x23	Float	R	Line frequency reading in Hz
0x24~0x25	Float	R	Reactive power reading in var
0x26~0x29	QWord	R	Reactive energy counter in varh
0x2a	Word	R	Residual current status: <ul style="list-style-type: none"> <li>• 0: Unknown</li> <li>• 1: Normal</li> <li>• 2: Warning</li> <li>• 3: Critical</li> <li>• 4: Self-Test</li> <li>• 5: Failure</li> </ul>
0x2b~0x2c	Float	R	Residual current reading in A
0x2d~0x2e	Float	R	Residual DC current reading in A
0x2f			Reserved